Off-Detector Calorimeter Digitizer electronics

- Function
- Past experience
- System block diagram
- ADC board block diagram, cable test result, differential receivers, ADC choice. Comments on trigger primitives
- Varies boards layout.
- Issue/Concern

Calorimeter Digitizer electronics function

- Digitizing the signal after the on-detector electronics with single scale 14 bit ADC.
  - Try to maintain the best dynamic range as good we can do with single scale ADC. We are looking for 12 bits dynamic range.
- Interface with PHENIX DAQ system
  - Receive beam clock, L0 timing and L1 trigger
  - Provide the 5 L1 trigger events buffer.
  - Provide the functionality to generate L1 trigger primitives.

Past Experience

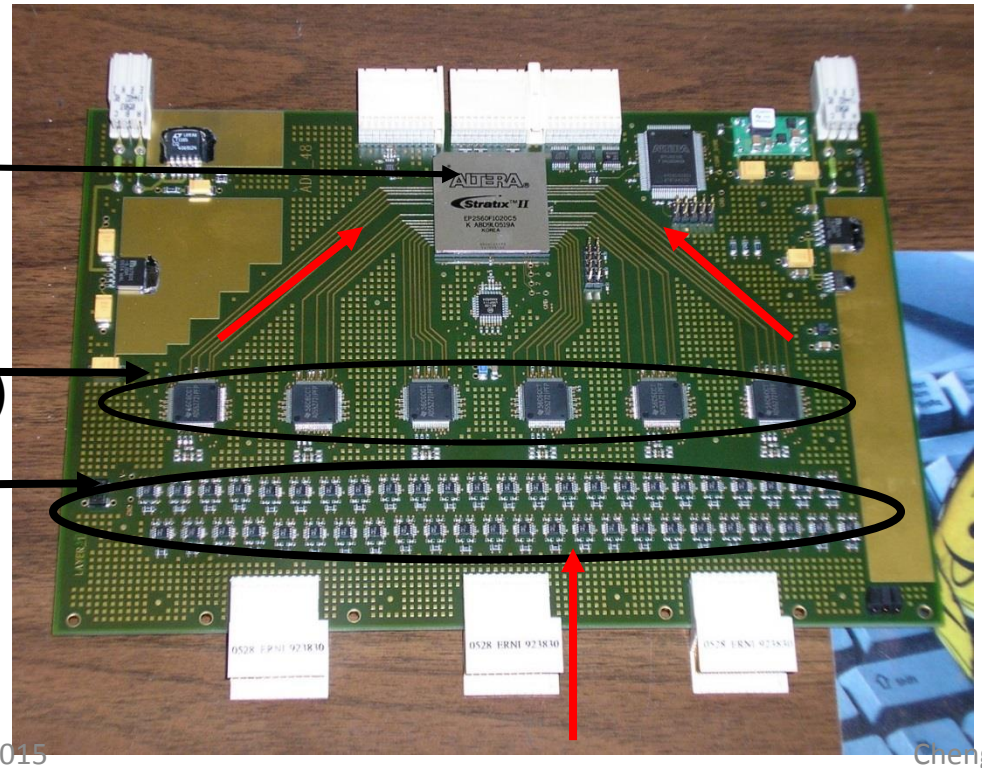
Built

PHENIX Hadron Blind Detector (HBD) off-detector digitizer (12 bits, 60 MHz)

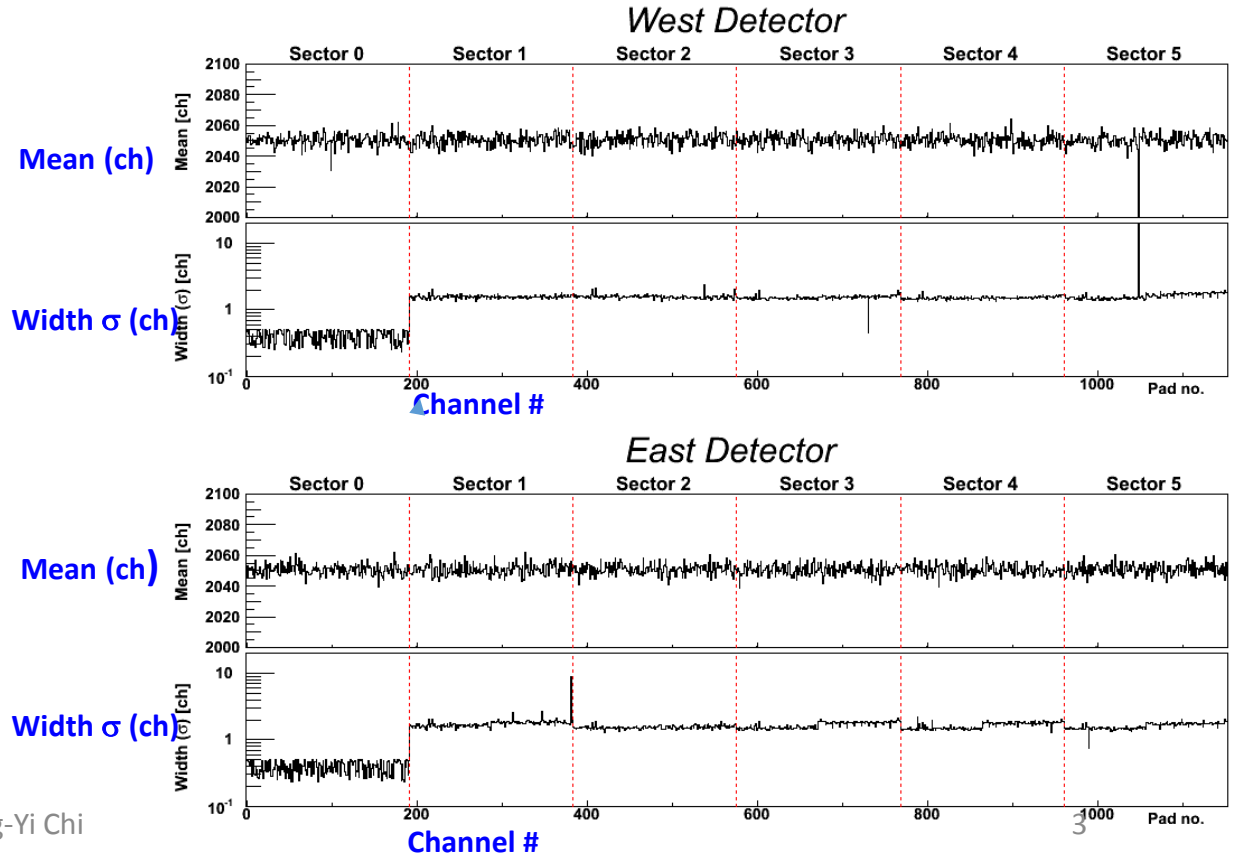
also been use for the MPC readout electronics and Sphenix test beam readout

MicroBoone TPC readout (BNL+Nevis) and PMT readout (similar shaper+ADC like HBD, 64 MHz)

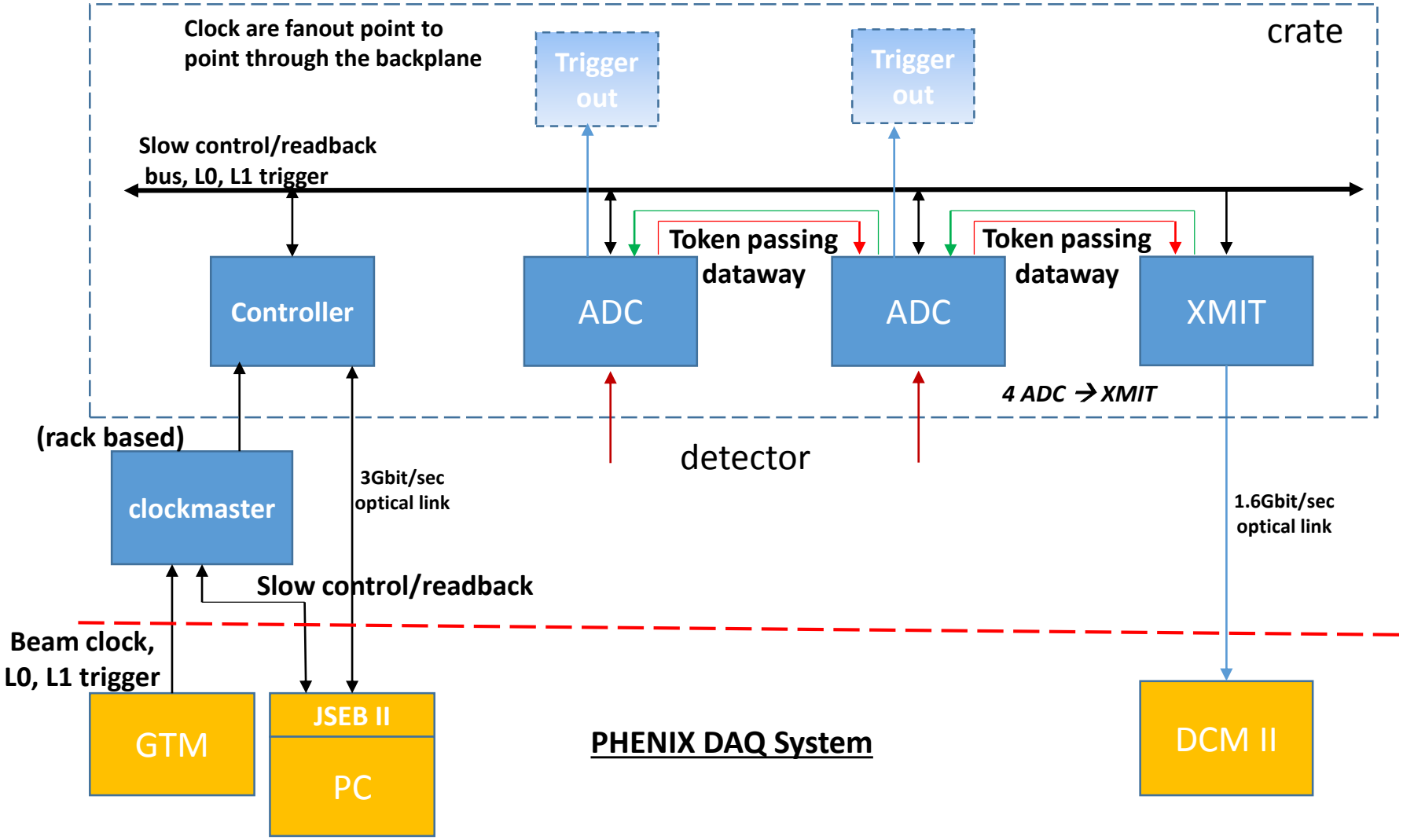
HBD ADC module



HBD Pedestal Run



ADC System Block Diagram



Crate based system.

Signals are cable from the on-detector electronics.

Digitized with 14 bit ADC.

Receive timing information the PHENIX Granule Timing Module (GTM)

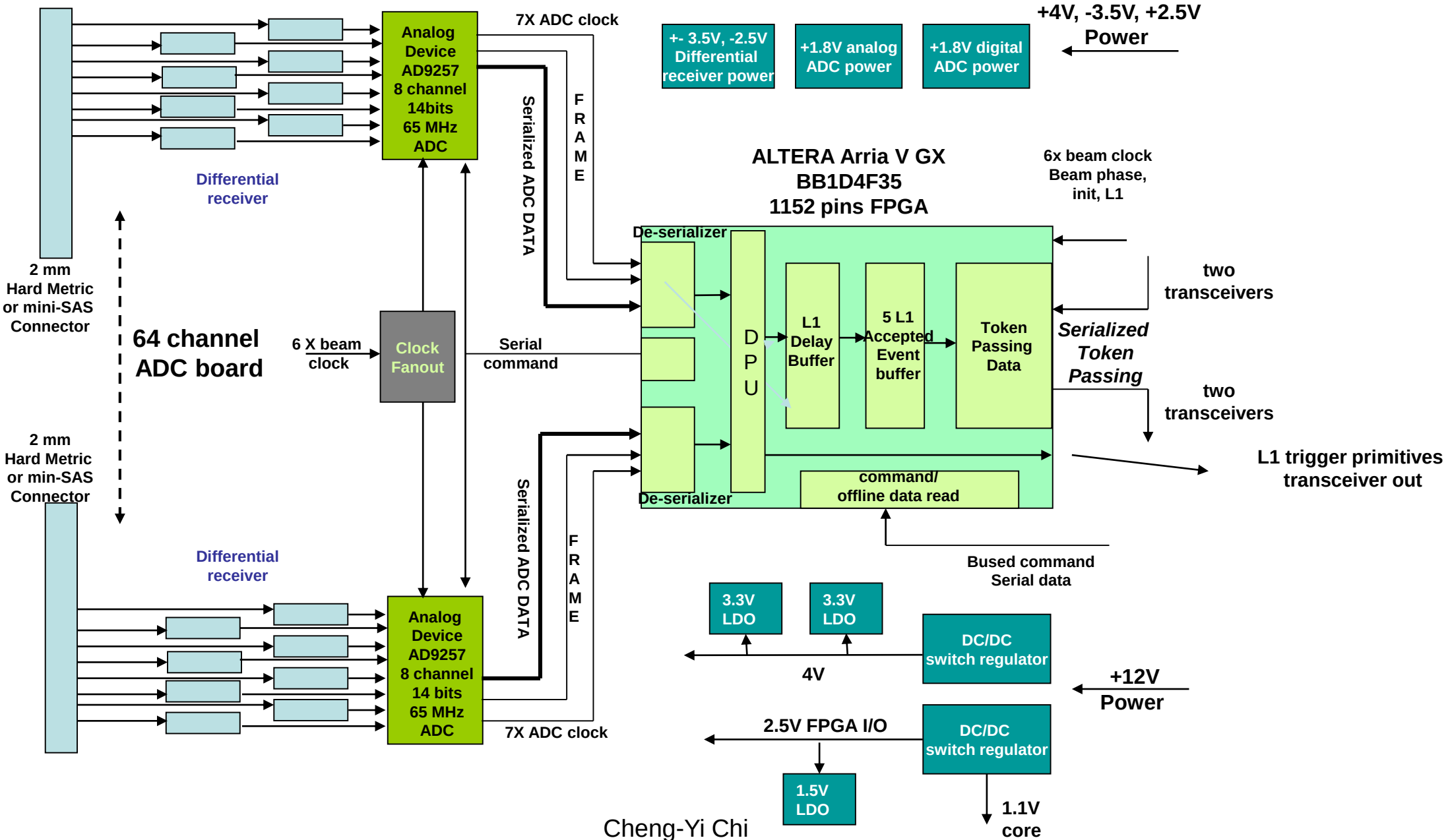
Generate L1 trigger primitives (not in the baseline scope)

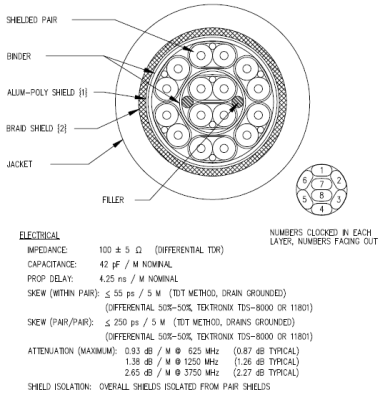
Receive L1 trigger and send out L1 triggered event data to Data Collection Module II (DCMII).

Provide buffer for both the 40 beam crossing L1 delay buffer and 5 L1 triggered events

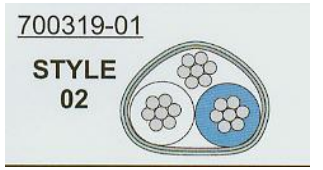
sPHENIX ADC Module Block Diagram

RHIC beam clock 9.6MHz

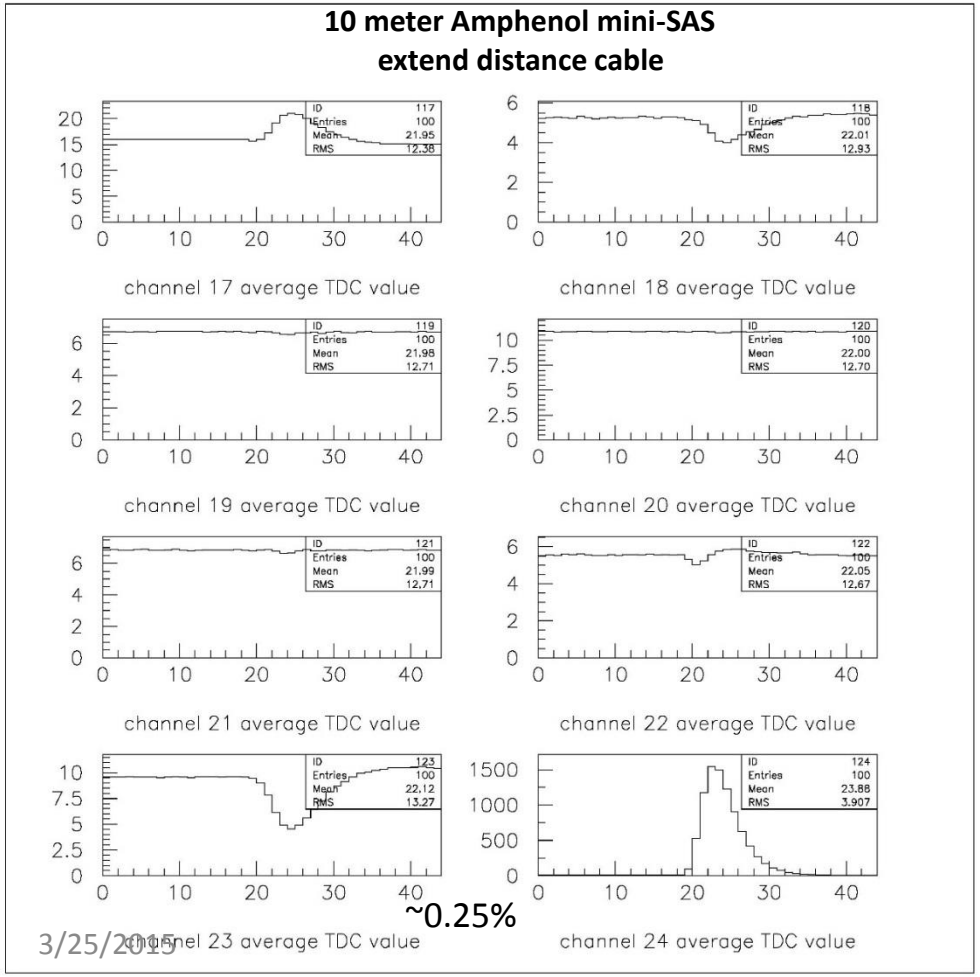




SPHENIX cable cross talk study

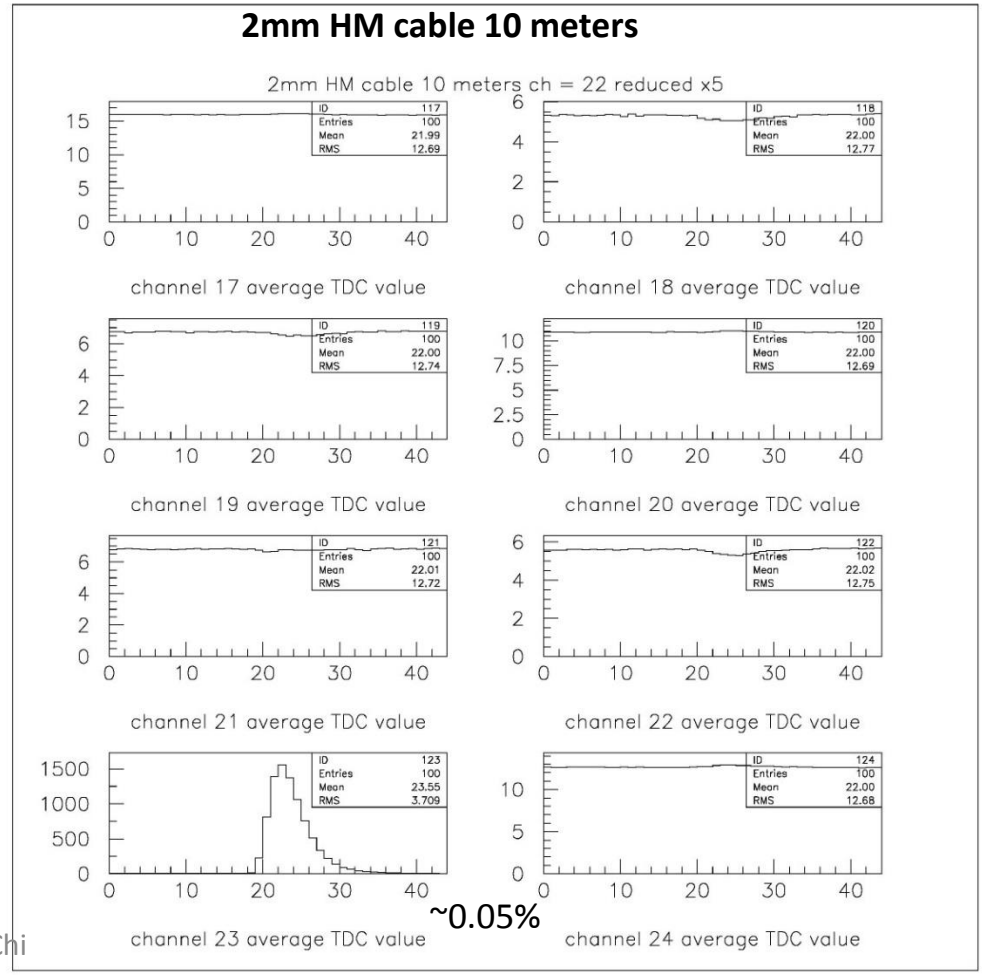


10 meter Amphenol mini-SAS extend distance cable

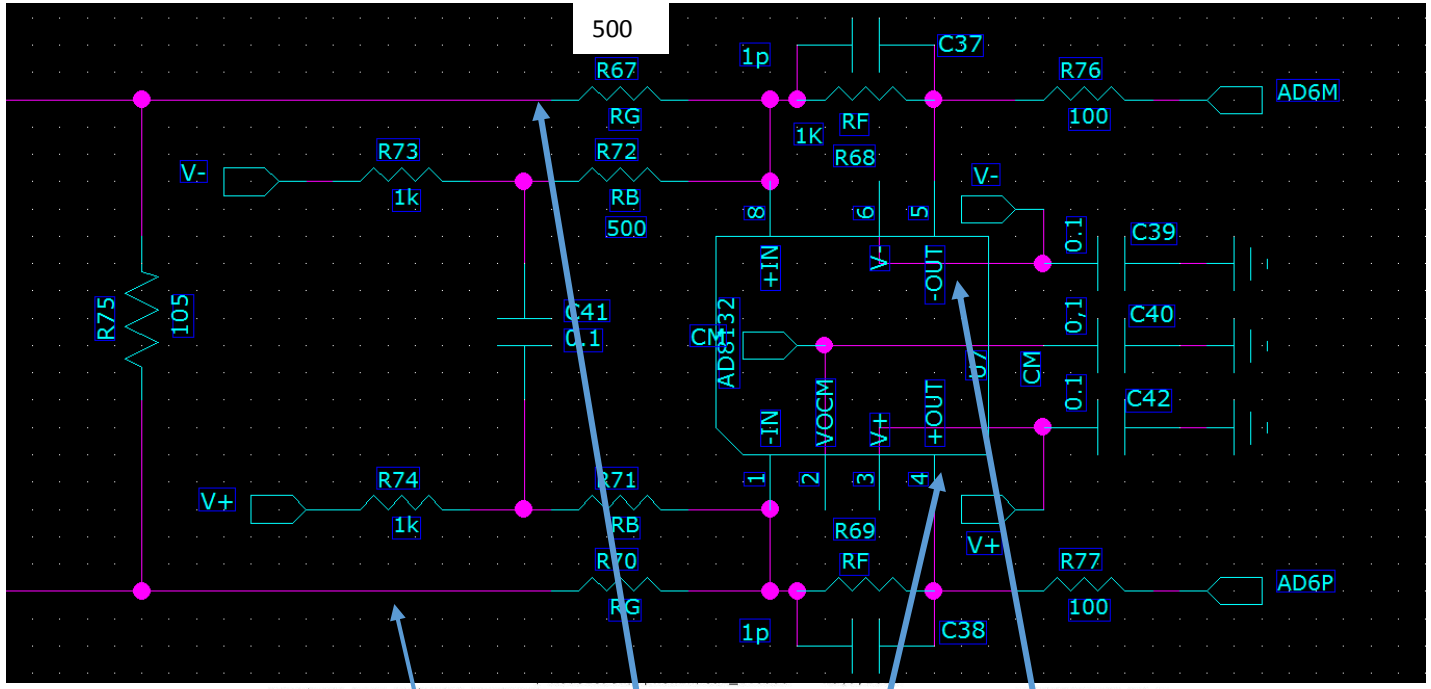


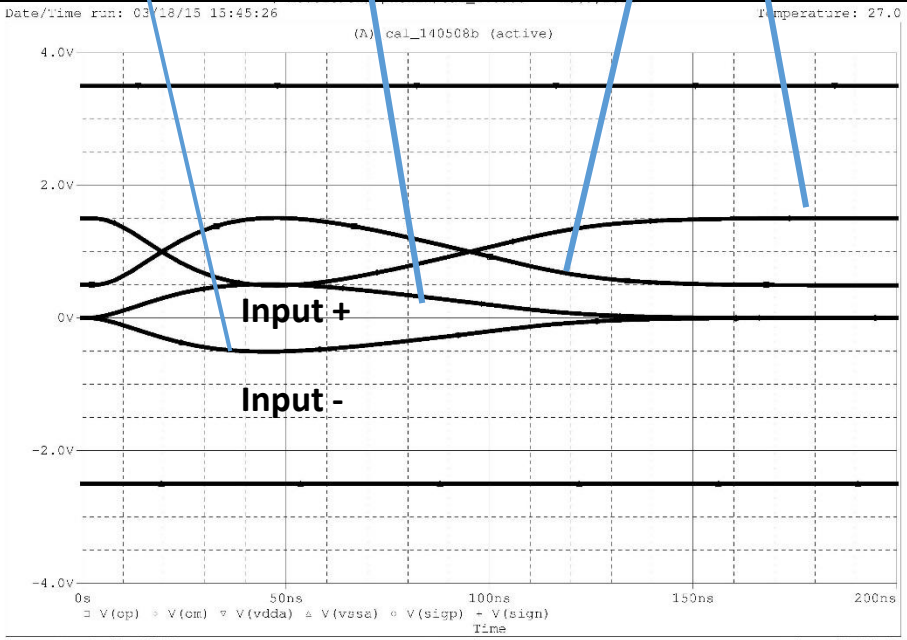
~0.25%

2mm HM cable 10 meters



~0.05%





V+

out-

out+

V-

Differential Receiver

The ADC module will receive the signal from the On detector module.

The signal will be AC coupled. The blocking capacitor will be on the frontend.

The ADC's Vcommon is at 1V. With the signal swing +-0.5v among Vcommon. To get full range of the ADC, the signal need to swing in both direction. The signal from the detector only swing in one direction.

We offset of the differential receiver to push the baseline to the lower ADC range.

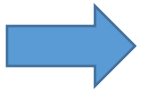
The resistors are discrete components. Supply voltages are adjustable through resistors.

The Choice of ADC

The limit of ADC LVDS serializer seems to be less than 1Gbits/sec
→ 65 MHZ ADC

The FPGA does not have 128 LVDS De-serializer → 1 LVDS output per ADC channel

JSED204B's ADC need the transceiver to receive data
→ Limits number of ADC can be connected to the reasonable price FPGA



Analog device AD9249

16 channel 14 bits ADC. Maximum sampling rate 65 MHz SNR 75db
1.8v technology. 58mw per channel at 65 MHz -> 1 W per chip.
144 pins package. 1cm X 1cm BGA
pipeline latency 16 clocks.

Analog Device **AD9257**

8 channel 14 bits ADC Maximum sampling rate 65 MHz SNR 75.5 db
1.8v technology. 55mw per channel at 65 MHz
65 pins LFCSP package. 0.9mm by 0.9mm.
pipeline latency 16 clocks.

Texas instrument ADS5294

8 channel 14 bits ADC. Maximum sampling rate 80 MHz SNR 75.5db
1.8v technology. Per channel 58mw at 50 MHz, 77mw at 80 MHz.
1-wire only interface only for below 50 MHz sampling
80 pins QFP package. 12mm by 12mm
included digital processing block (only after digitization)
pipeline latency 11 clocks for 1 wire interface.

Linear Technology LTM9008-14

8 channel 14 bits ADC. Maximum sampling rate 65MHz SNR 73 db
1.8v technology. Per channel 88mw at 65 MHz.
140 pins BGA. 11.25mm X 9mm
pipeline latency 6 clocks.

Thoughts on the Trigger Primitives.

FEM can do rough gain correction → We will do on board 2x2 sum first
If trigger primitive output will be 8 bits, for 40 Gev top scale, the least count
will be ~156 Mev if the scale is linear.

If we output 8 bits per channels, the optical bandwidth will be 10 (8b/10b encoding) *64 * 10 MHz = 6.4 Gbits/sec. if one only output 2X2 sum, we will only have 1.6 Gbits/sec. With formatting, the output will be 2 Gbits/sec. (1 frame marker + 1 header + 8* (2* 8) data words.)

if trigger sum is 10 bits, we will have (1 frame marker + 1 header + 10 16 bits data words.), The optical Bandwidth will be 20 (bits)*12 words* 10 MHz = 2.4 Gbits/sec

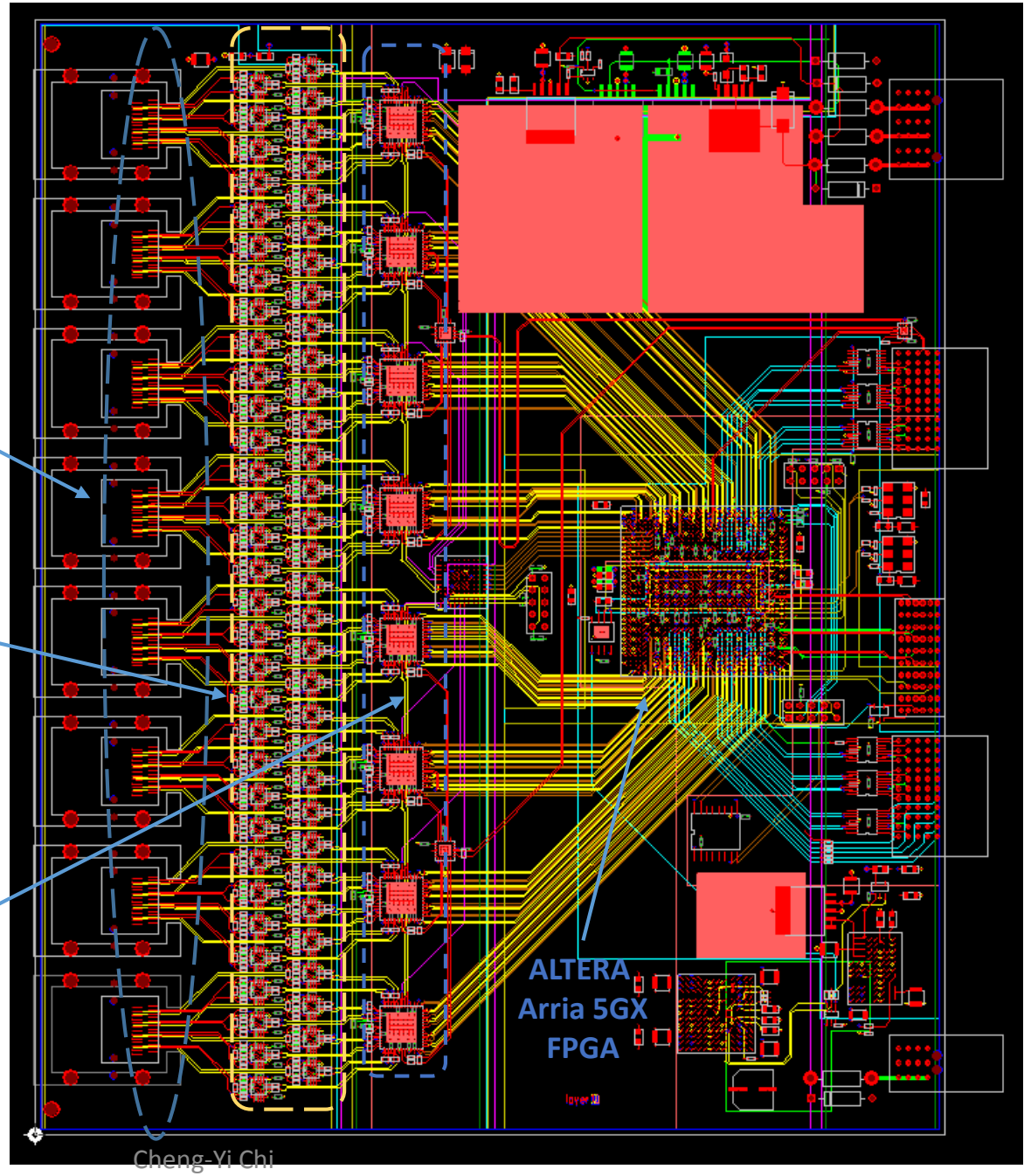
sPHENIX ADC board

64 channel inputs
Mini-SAS / 2mm HM connectors
160mm by 190mm (6U board)

The 8 channel 14 bits ADC will be running at 6x beam crossing rate ~ 60 MHz

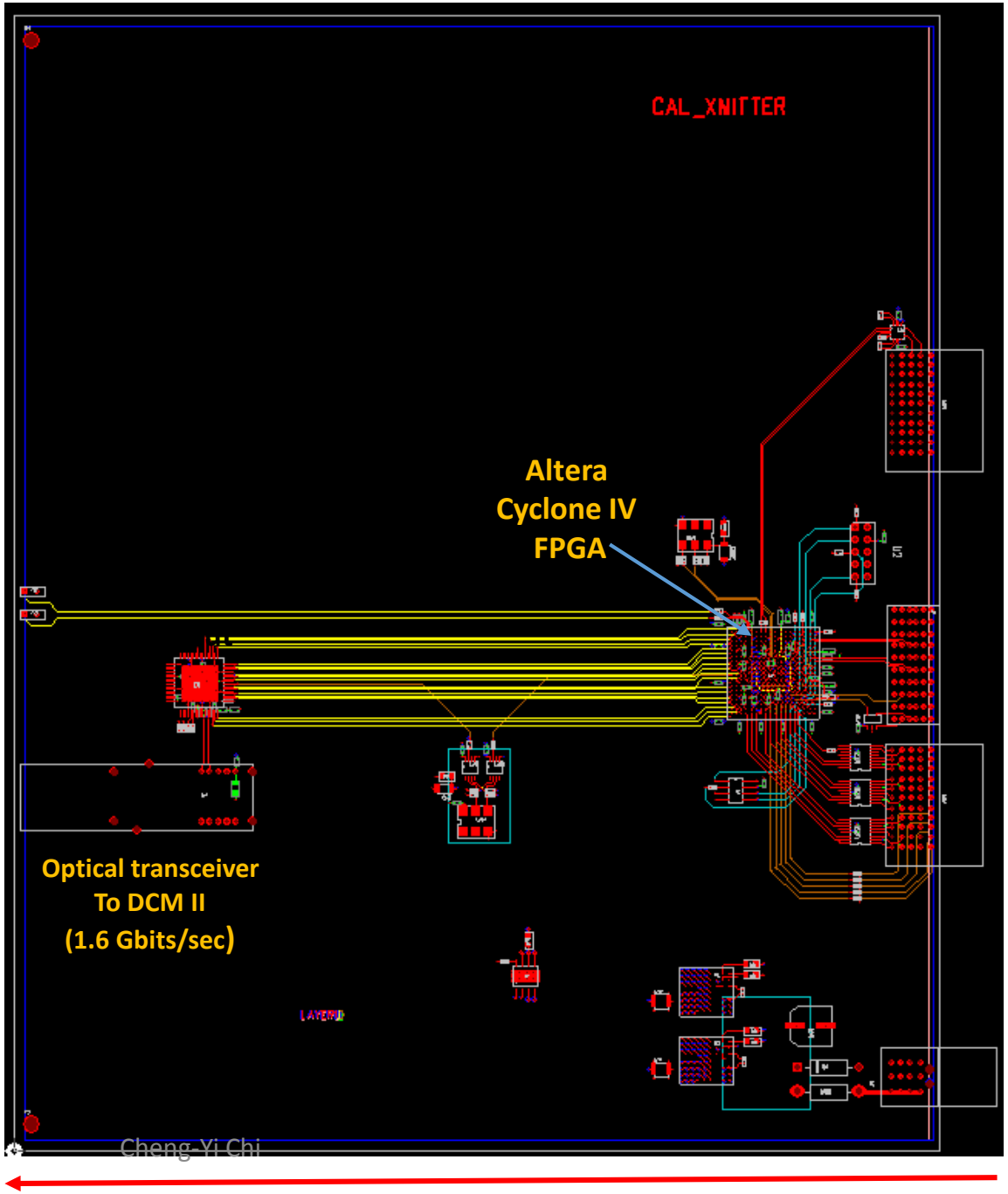
Altera Arria 5GX FPGA de-serialize data, provide 5 events buffer, 40 beam crossing L1 delay, token passing data, L1 trigger primitives output

Will do a version of 2mm HM connector → 1st choice.

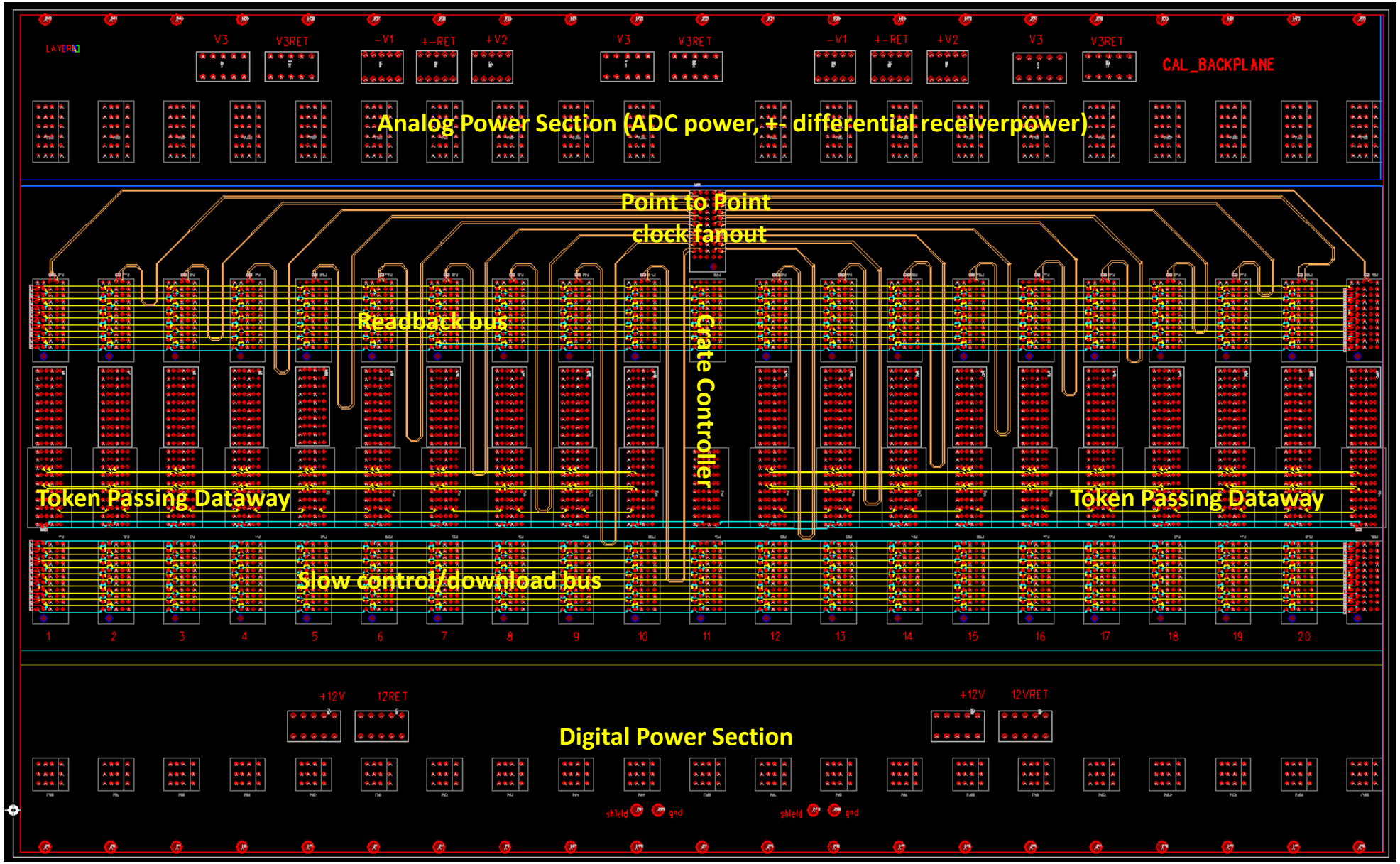


XMIT Module

. Receive data from FEM
. Issue token after receive all data transfer
. Format FEM data (header and checksum)
. Error handling



Crate Backplane



Crate Controller

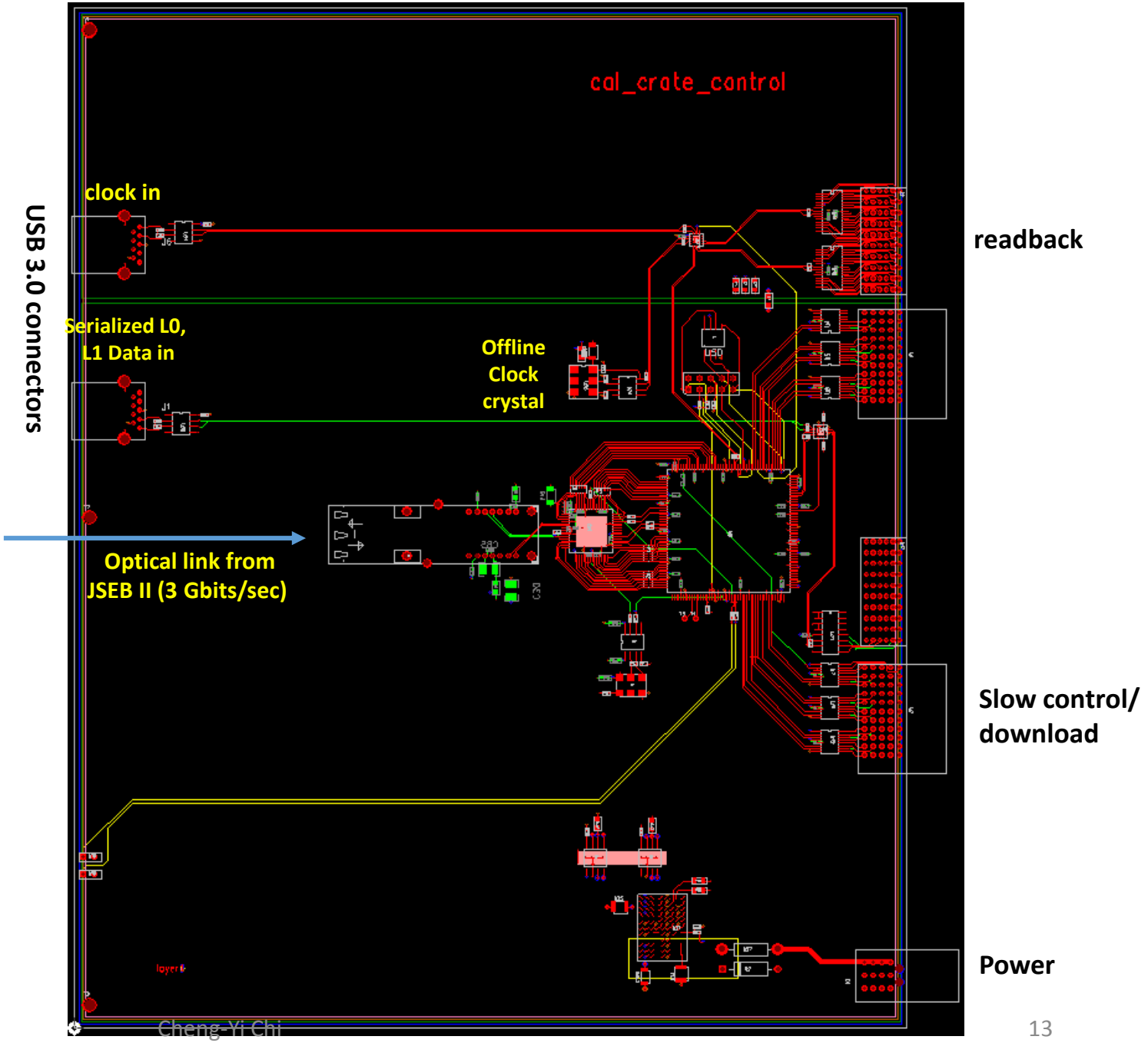
Receive clock and L0 (init, test etc), L1 trigger.

Receive slowdown load from DAQ system.

- Write ADC's module FPGA boot code to the EPROM.
- Write ADC, XMIT & Controller modules running parameters.
- Download varies table.
- Download fake data
- Initialize system. Set online/offline system

Provide offline clock/L0 data, L1 trigger. (standalone crate running)

Provide readback from ADC module to computer.



Issues/Concern

- We have 1st design for all the major boards.
  - ADC, XMIT, Controller and Backplane. The clockmaster boards is not required for the 1st round prototype.
  - Now we need to iterate the design to make a consistent flow
  - Checking and revision is now in progress.
  - We expect 1-2 months of checking and ordering parts before submitting the design to the fabrication. It also takes time to get order processed.
  - If everything go smoothly we will have a working prototype in later 2015.
    - Many questions need to be addressed both on the analog and digital fronts.
  - Need to give some thoughts on the trigger primitive output testing.